Patent Application
Attorney Docket No.: 57941.000037
Client Reference No.: RA208.P.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Jared Zerbe, et al.	:	Group Art Unit: 2863
	:	
Appln. No.: 09/776,550	:	
	:	Examiner: Tung S. Lau
Filed: February 2, 2001	:	
	:	
For: METHOD AND APPARATUS FOR EVALUATING AND CALIBRATING A SIGNALING SYSTEM	:	

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL

Sir:

Submitted herewith is an Appeal Brief for the above-identified patent application.

[ ] No additional fee is required.

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	PRESENT # OF CLAIMS	HIGHEST # PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	21	21	0	x $18 =	$.00
Independent Claims	2	3	0	x $86 =	$.00
				Subtotal	$.00
				Subtract ½ if Small Entity	$.00
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Respectfully submitted,

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Date: May 17, 2004

IFW AF/8

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed March 17, 2004.

REAL PARTY IN INTEREST

The Appellants, Jared Zerbe, Pak Shing Chau, and William Franklin Stonecypher, are the Applicants in the above-identified patent application. The Appellants have assigned their entire interest in the above-identified patent application to Rambus Inc., 4440 El Camino Real, Los Altos, California 94022.

RELATED APPEALS AND INTERFERENCES

The Appellants, the Appellants' legal representative, and the Assignee are not aware of any other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this Appeal.

STATUS OF CLAIMS

Claims 1-21 are pending in the above-identified patent application. Claims 4, 5, 11, 13, and 19-21 were indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-3, 6-10, 12, and 14-18 were finally rejected in an Office Action dated November 20, 2003. The final rejection of Claims 1-3, 6-10, 12, and 14-18 is hereby appealed.

Claims 1-3, 6-10, 12, and 14-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Gruetzner et al. (U.S. Patent No. 5,444,715).

STATUS OF AMENDMENTS

No claim amendments have been filed subsequent to the Final Office Action issued on November 20, 2003.

SUMMARY OF INVENTION

The claimed invention, as set forth in claim 1, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, is directed to a digital signaling system (e.g., see Figures 1 and 23; page 9, line 12, through page 12, line 6; page 34, line 24, through page 35, line 15) comprising a transmit circuit (e.g., transmit circuit 101 in Figure 1) and a receive circuit (e.g., receive circuit 103 in Figure 1). The transmit circuit may comprise a transmit data input (e.g., data input 104 in Figure 1) and a transmit data output (e.g., medium 102 in Figure 1). The transmit circuit may produce a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode. The transmit circuit may further comprise a transmit repeating pattern generator (e.g., shift register 105 and test loop 106 in Figure 1) producing a repeating pattern signal. The transmit circuit may produce the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode.

The receive circuit, which is operably coupled to the transmit circuit, may receive the transmit data output signal

from the transmit circuit at a receive data input (e.g., medium 102 in Figure 1). The receive circuit may comprise a receive data output (e.g., data output 109 in Figure 1). The receive circuit may produce a receive data output signal at the receive data output based on the transmit data output signal when the receive circuit is operating in the normal mode. The receive circuit may further comprise a receive repeating pattern generator (e.g., shift register 108 and test loop 111 in Figure 1) producing the repeating pattern signal. The receive circuit may also produce a comparison signal (e.g., comparison output 114 in Figure 1) based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode.

The claimed invention, as set forth in claim 2, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by the transmit repeating pattern generator comprising a transmit shift register (e.g., shift register 105 in Figure 1) and the receive repeating pattern generator comprising a receive shift register (e.g., shift register 108 in Figure 1).

The claimed invention, as set forth in claim 3, and as described and shown in the specification and Figures 1-31 of the

above-identified patent application, respectively, may be further defined by a transmit shift register output of the transmit shift register (e.g., shift register 105 in Figure 1) being coupled to a transmit shift register input of the transmit shift register when the transmit circuit (e.g., transmit circuit 101 in Figure 1) is operating in the test mode, and a receive shift register output of the receive shift register being coupled to a receive shift register input of the receive shift register (e.g., shift register 108 in Figure 1) when the receive circuit (e.g., receive circuit 103 in Figure 1) is operating in the test mode.

The claimed invention, as set forth in claim 6, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by the transmit data output signal being capable of representing two bits of information simultaneously over a single conductor (e.g., medium 102 in Figure 1; page 9, lines 6-10; Figure 23; page 35, lines 5-6).

The claimed invention, as set forth in claim 7, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by the transmit data output signal being communicated over a single conductor referenced to a ground

voltage (e.g., medium 102 in Figure 1; page 9, lines 6-10; Figure 23; page 35, lines 3-4).

The claimed invention, as set forth in claim 8, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by the transmit data output signal being communicated as a differential signal over two conductors (e.g., medium 102 in Figure 1; page 9, lines 6-10; Figure 23; page 35, lines 4-5).

The claimed invention, as set forth in claim 9, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, is also directed to a method for evaluating a digital signaling system (e.g., see Figures 1 and 23; page 9, line 12, through page 12, line 6; page 34, line 24, through page 35, line 15) comprising generating a transmit repeating pattern in a transmit circuit (e.g., transmit circuit 101 in Figure 1), transmitting the transmit repeating pattern to a receive circuit (e.g., to receive circuit 103 via medium 102 in Figure 1), generating a receive repeating pattern in the receive circuit (e.g., via shift register 108 and test loop 111 in Figure 1), and comparing the transmit repeating pattern to the receive repeating pattern

to obtain a comparison (e.g., comparison output 114 in Figure 1).

The claimed invention, as set forth in claim 10, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by adjusting a parameter affecting operation of the transmit circuit based on the comparison (e.g., Figure 23; page 34, line 24, through page 35, line 15).

The claimed invention, as set forth in claim 12, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by utilizing a shift register (e.g., shift register 105 in Figure 1) to generate the transmit repeating pattern (e.g., Figure 23; page 34, line 24, through page 35, line 15).

The claimed invention, as set forth in claim 14, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by transmitting the transmit repeating pattern as a signal referenced to a ground (e.g., medium 102 in Figure 1; page 9, lines 6-10; Figure 23; page 35, lines 3-4).

The claimed invention, as set forth in claim 15, and as described and shown in the specification and Figures 1-31 of the

above-identified patent application, respectively, may be further defined by transmitting the transmit repeating pattern as a differential signal over a pair of conductors (e.g., medium 102 in Figure 1; page 9, lines 6-10; Figure 23; page 35, lines 4-5).

The claimed invention, as set forth in claim 16, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously (e.g., medium 102 in Figure 1; page 9, lines 6-10; Figure 23; page 35, lines 5-6).

The claimed invention, as set forth in claim 17, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by adjusting a receiver characteristic of the receive circuit (e.g., page 8, line 29, through page 9, line 1; page 12, lines 1-6).

The claimed invention, as set forth in claim 18, and as described and shown in the specification and Figures 1-31 of the above-identified patent application, respectively, may be further defined by the receiver characteristic being selected

from a group consisting of a receiver circuit timing signal and a voltage reference (e.g., page 12, lines 1-6).

ISSUES

Whether claims 1-3, 6-10, 12, and 14-18 are anticipated by Gruetzner et al. (U.S. Patent No. 5,444,715) under 35 U.S.C. § 102(b).

GROUPING OF CLAIMS

Claim 1 is an independent system claim directed to digital signaling system. Claims 2, 3, and 6-8 are dependent from claim 1. Thus, claims 2, 3, and 6-8 all stand with claim 1.

Claim 9 is an independent method claim directed to a method for evaluating a digital signaling system. Claims 10, 12, and 14-18 are dependent from claim 9. Thus, claims 10, 12, and 14-18 all stand with claim 9.

Claims 6 and 16, claims 7 and 14, and claims 8 and 15 are all of similar scope. Thus, claims 6 and 16, claims 7 and 14, and claims 8 and 15 fall together. All other claims fall by themselves.

ARGUMENT

The Appellants respectfully appeal the decision of the Examiner to finally reject claims 1-3, 6-10, 12, and 14-18 of the present application. As discussed below, it is respectfully submitted that the Examiner has failed to establish a prima facie case of anticipation against the appealed claims.

I. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d

1955, 1957 (Fed. Cir. 1993). "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claim 1, the Examiner asserts that Gruetzner et al. teach a transmit circuit, the transmit circuit comprising a transmit data input and a transmit data output, the transmit circuit producing a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode (the Examiner refers to column 4, lines 25-53; and Figure 1, items 111 and 127). However, item 111 in Figure 1 of Gruetzner et al. is specifically described as a receiving circuit, and item 127 in Figure 1 of Gruetzner et al. is specifically described as an output of the receiving circuit. This is obviously in contrast to the present claim language,

which is directed specifically to a transmit circuit. Accordingly, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to a transmit circuit comprising a transmit data input and a transmit data output, wherein the transmit circuit produces a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode, as claimed.

The Examiner also asserts that Gruetzner et al. teach the transmit circuit further comprising a transmit repeating pattern generator producing a repeating pattern signal, the transmit circuit producing the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode (the Examiner refers to columns 2-3, lines 49-38; column 4, lines 25-53; and Figure 2). However, it is respectfully submitted that Gruetzner et al. do not disclose or even suggest a transmit repeating pattern generator producing a repeating pattern signal, as claimed. In fact, the closest Gruetzner et al. come to teaching a transmit repeating pattern generator for producing a repeating

pattern signal is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of a transmit repeating pattern generator producing a repeating pattern signal, as claimed. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to a transmit circuit further comprising a transmit repeating pattern generator producing a repeating pattern signal, wherein the transmit circuit produces the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode, as claimed.

Similarly, the Examiner further asserts that Gruetzner et al. teach a receive circuit comprising a receive repeating pattern generator producing a repeating pattern signal, the receive circuit producing a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode (the Examiner refers to columns 2-3, lines 49-38; column 4, lines 25-53; and Figure 2). However, it is

respectfully submitted that Gruetzner et al. do not disclose or even suggest a receive repeating pattern generator producing a repeating pattern signal, as claimed. In fact, the closest Gruetzner et al. come to teaching a receive repeating pattern generator for producing a repeating pattern signal is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of a receive repeating pattern generator producing a repeating pattern signal as claimed. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to a receive circuit comprising a receive repeating pattern generator producing a repeating pattern signal, wherein the receive circuit produces a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode, as claimed.

Accordingly, it is respectfully submitted that Gruetzner et al. does not anticipate claim 1 of the present application.

Regarding claims 2, 3, and 6-8, these claims are dependent

upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2, 3, and 6-8 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by Gruetzner et al. or any of the other cited references taken either alone or in combination. For example, claim 2 recites that the transmit repeating pattern generator comprises a transmit shift register and the receive repeating pattern generator comprises a receive shift register. The Examiner asserts that Gruetzner et al. teach that a repeating pattern generator may be implemented by a shift register (the Examiner refers to columns 2-3, lines 49-37). However, since Gruetzner et al. do not even teach a repeating pattern generator, as discussed above, Gruetzner et al. can not teach a repeating pattern generator being implemented by a shift register. Furthermore, the context in which Gruetzner et al. discuss shift registers is such that the shift registers are used for shifting arbitrary test data (see column 3, lines 4-6), not for producing a repeating pattern signal, as claimed. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number,

column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to a transmit repeating pattern generator comprising a transmit shift register and a receive repeating pattern generator comprising a receive shift register, as claimed.

Also, claim 3 recites that a transmit shift register output of the transmit shift register is coupled to a transmit shift register input of the transmit shift register when the transmit circuit is operating in the test mode, and that a receive shift register output of the receive shift register is coupled to a receive shift register input of the receive shift register when the receive circuit is operating in the test mode. The Examiner asserts that Gruetzner et al. teach this limitation at columns 3-4, lines 49-37. However, since Gruetzner et al. do not even teach a repeating pattern generator, as discussed above, Gruetzner et al. can not teach a repeating pattern generator being implemented by a shift register. Furthermore, it is respectfully submitted that Gruetzner et al. do not claim, disclose, or even suggest the claimed coupling arrangement (i.e., shift register outputs being coupled to shift register inputs when operating in test mode). Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing

identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to a transmit shift register output of a transmit shift register coupled to a transmit shift register input of the transmit shift register when the transmit circuit is operating in the test mode, and a receive shift register output of a receive shift register coupled to a receive shift register input of the receive shift register when the receive circuit is operating in the test mode, as claimed.

Furthermore, claim 6 recites that the transmit data output signal is capable of representing two bits of information simultaneously over a single conductor. The Examiner asserts that item 124 in Figure 1 and Figure 2 of Gruetzner et al. teach this limitation. However, item 124 in Figure 1 of Gruetzner et al. is merely disclosed to be a line interconnecting sending chip 110 and receiving chip 111. Nowhere do Gruetzner et al. claim, disclose, or even suggest that a transmit data output signal is capable of representing two bits of information simultaneously over a single conductor. In fact, it is respectfully submitted that Gruetzner et al. cannot even support such a feature, which requires multi-level signaling capability. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of

anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that allow the transmit data output signal to represent two bits of information simultaneously over a single conductor, as claimed.

Furthermore, claim 8 recites that the transmit data output signal is communicated as a differential signal over two conductors. The Examiner asserts that items 120 and 121 in Figure 1 of Gruetzner et al. teach this limitation. However, items 120 and 121 in Figure 1 of Gruetzner et al. are merely disclosed to be lines interconnecting two separate master/slave devices 114 and 115 to a driver 122. Nowhere do Gruetzner et al. claim, disclose, or even suggest that a transmit data output signal is communicated as a differential signal over two conductors. In fact, it is respectfully submitted that Gruetzner et al. cannot even support such a feature, which requires differential transmitters and receivers. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that allow the transmit data output signal to be communicated as a differential signal over two conductors, as claimed.

Accordingly, it is respectfully submitted that Gruetzner et al. do not anticipate claims 2, 3, and 6-8 of the present application.

Regarding claim 9, the Examiner asserts that Gruetzner et al. teach generating a transmit repeating pattern in a transmit circuit, and transmitting the transmit repeating pattern to a receive circuit (the Examiner refers to column 1 , lines 35-57; columns 2-3, lines 49-38). However, it is respectfully submitted that Gruetzner et al. do not disclose or even suggest generating a transmit repeating pattern in a transmit circuit, and transmitting the transmit repeating pattern to a receive circuit, as claimed. In fact, the closest Gruetzner et al. come to teaching generating a transmit repeating pattern in a transmit circuit is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of generating a transmit repeating pattern in a transmit circuit, as claimed. Furthermore, the Examiner refers to column 1 , lines 35-57, of Gruetzner et al. to support his assertion, but this teaching (see column 1, lines 54-57) is specifically limited to testing individual chips (i.e., not interconnections between chips (e.g., systems)), which is totally in contrast to the present

invention, as claimed. Thus, Gruetzner et al. actually teach away from the present invention as claimed, since, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The Examiner also asserts that Gruetzner et al. teach generating a receive repeating pattern in the receive circuit, and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison (the Examiner refers to column 1, lines 35-57; columns 2-3, lines 49-38). However, it is respectfully submitted that Gruetzner et al. do not disclose or even suggest generating a receive repeating pattern in the receive circuit, and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison, as claimed. In fact, the closest Gruetzner et al. come to teaching generating a receive repeating pattern in the receive circuit is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of generating a receive repeating pattern in the receive circuit, as claimed. Furthermore, the Examiner

refers to column 1 , lines 35-57, of Gruetzner et al. to support his assertion, but this teaching (see column 1, lines 54-57) is specifically limited to testing individual chips (i.e., not interconnections between chips (e.g., systems)), which is totally in contrast to the present invention as claimed. Thus, Gruetzner et al. actually teach away from the present invention as claimed, since, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Accordingly, it is respectfully submitted that Gruetzner et al. does not anticipate claim 9 of the present application.

Regarding claims 10, 12, and 14-18, these claims are dependent upon independent claim 9. Thus, since independent claim 9 should be allowable as discussed above, claims 10, 12, and 14-18 should also be allowable at least by virtue of their dependency on independent claim 9. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by Gruetzner et al. or any of the other cited references taken either alone or in combination. For example, claim 10 recites adjusting a parameter affecting operation of

the transmit circuit based on the comparison. The Examiner asserts that Gruetzner et al. teach adjusting a parameter affecting operation of the transmit circuit based on the comparison (the Examiner refers to column 1, lines 35-57; columns 2-3, lines 20-37; the abstract; and items 110 and 111 in Figure). However, Applicants could find no such teaching at column 1, lines 35-57, or anywhere else, of Gruetzner et al., particularly when the adjustment is based upon a comparison as required in claim 10. Thus, it is respectfully submitted that Gruetzner et al. fail to teach adjusting a parameter affecting operation of the transmit circuit based on the comparison, as claimed. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to adjusting a parameter affecting operation of the transmit circuit based on the comparison, as claimed.

Also, claim 12 recites utilizing a shift register to generate the transmit repeating pattern. The Examiner asserts that Gruetzner et al. teach that a transmit repeating pattern may be generated by a shift register (the Examiner refers to columns 2-3, lines 49-37). However, since Gruetzner et al. do

not even teach generating a transmit repeating pattern, as discussed above, Gruetzner et al. can not teach utilizing a shift register to generate the transmit repeating pattern. Furthermore, the context in which Gruetzner et al. discuss shift registers is such that the shift registers are used for shifting arbitrary test data (see column 3, lines 4-6), not for producing a repeating pattern signal, as claimed. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to utilizing a shift register to generate the transmit repeating pattern, as claimed.

Furthermore, claim 14 recites transmitting the transmit repeating pattern as a signal referenced to a ground. The Examiner does not even address how this claim is anticipated by Gruetzner et al.. However, since Gruetzner et al. do not even teach generating a transmit repeating pattern, as discussed above, Gruetzner et al. can not teach transmitting the transmit repeating pattern as a signal referenced to a ground. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number,

column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to transmitting the transmit repeating pattern as a signal referenced to a ground, as claimed.

Furthermore, claim 15 recites transmitting the transmit repeating pattern as a differential signal over a pair of conductors. The Examiner asserts that items 120 and 121 in Figure 1 of Gruetzner et al. teach this limitation. However, items 120 and 121 in Figure 1 of Gruetzner et al. are merely disclosed to be lines interconnecting two separate master/slave devices 114 and 115 to a driver 122. Nowhere do Gruetzner et al. claim, disclose, or even suggest transmitting the transmit repeating pattern as a differential signal over a pair of conductors. In fact, it is respectfully submitted that Gruetzner et al. cannot even support such a feature, which requires differential transmitters and receivers. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to transmitting the transmit repeating pattern as a differential signal over a pair of conductors, as claimed.

Furthermore, claim 16 recites transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously. The Examiner asserts that item 124 in Figure 1 and Figure 2 of Gruetzner et al. teach this limitation. However, item 124 in Figure 1 of Gruetzner et al. is merely disclosed to be a line interconnecting sending chip 110 and receiving chip 111. Nowhere do Gruetzner et al. claim, disclose, or even suggest transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously. In fact, it is respectfully submitted that Gruetzner et al. cannot even support such a feature, which requires multi-level signaling capability. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously, as claimed.

Furthermore, claim 17 recites adjusting a receiver characteristic of the receive circuit. The Examiner asserts that Gruetzner et al. teach adjusting a receiver characteristic of the receive circuit (the Examiner refers to column 1, lines

35-57; columns 2-3, lines 20-37; the abstract; and items 110 and 111 in Figure). However, Applicants could find no such teaching at column 1, lines 35-57, or anywhere else, of Gruetzner et al.. Thus, it is respectfully submitted that Gruetzner et al. fail to teach adjusting a receiver characteristic of the receive circuit, as claimed. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that correspond to adjusting a receiver characteristic of the receive circuit, as claimed.

Furthermore, claim 18 recites that the receiver characteristic is selected from a group consisting of a receiver circuit timing signal and a voltage reference. The Examiner does not even address how this claim is anticipated by Gruetzner et al.. However, since Gruetzner et al. do not even teach adjusting a receiver characteristic of the receive circuit, as discussed above, Gruetzner et al. can not teach the receiver characteristic is selected from a group consisting of a receiver circuit timing signal and a voltage reference. Thus, again, Applicants respectfully submit that the Examiner has failed in his duty to present at least a prima facie case of anticipation

by failing to identify (e.g., by reference number, column and line number, etc.) the exact component(s) in Gruetzner et al. that allows for the receiver characteristic to be selected from a group consisting of a receiver circuit timing signal and a voltage reference, as claimed.

Accordingly, it is respectfully submitted that Gruetzner et al. does not anticipate claims 10, 12, and 14-18 of the present application.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner has failed to establish a prima facie case of anticipation against the appealed claims. Thus, it is respectfully submitted that the final rejection of claims 1-3, 6-10, 12, and 14-18 under 35 U.S.C. § 102(b) is improper and the reversal of same is clearly in order and respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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APPENDIX

1 (Previously Presented). A digital signaling system comprising:

a transmit circuit, the transmit circuit comprising a transmit data input and a transmit data output, the transmit circuit producing a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode, the transmit circuit further comprising a transmit repeating pattern generator producing a repeating pattern signal, the transmit circuit producing the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode; and

a receive circuit, the receive circuit operably coupled to the transmit circuit and receiving the transmit data output signal from the transmit circuit at a receive data input, the receive circuit comprising a receive data output, the receive circuit producing a receive data output signal at the receive data output based on the transmit data output signal when the receive circuit is operating in the normal mode, the receive circuit further comprising a receive repeating pattern generator producing the repeating pattern signal, the receive circuit

producing a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode.

2 (Original). The digital signaling system of claim 1 wherein the transmit repeating pattern generator comprises a transmit shift register and the receive repeating pattern generator comprises a receive shift register.

3 (Previously Presented). The digital signaling system of claim 2 wherein a transmit shift register output of the transmit shift register is coupled to a transmit shift register input of the transmit shift register when the transmit circuit is operating in the test mode and a receive shift register output of the receive shift register is coupled to a receive shift register input of the receive shift register when the receive circuit is operating in the test mode.

6 (Original). The digital signaling system of claim 1 wherein the transmit data output signal is capable of representing two bits of information simultaneously over a single conductor.

7 (Original). The digital signaling system of claim 1 wherein

the transmit data output signal is communicated over a single conductor referenced to a ground voltage.

8 (Original). The digital signaling system of claim 1 wherein the transmit data output signal is communicated as a differential signal over two conductors.

9 (Original). A method for evaluating a digital signaling system comprising the steps of:

generating a transmit repeating pattern in a transmit circuit;

transmitting the transmit repeating pattern to a receive circuit;

generating a receive repeating pattern in the receive circuit; and

comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison.

10 (Original). The method of claim 9 further comprising the steps of:

adjusting a parameter affecting operation of the transmit circuit based on the comparison.

12 (Original). The method of claim 9 wherein the step of generating a transmit repeating pattern in a transmit circuit comprises the step of:

utilizing a shift register to generate the transmit repeating pattern.

14 (Original). The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a signal referenced to a ground.

15 (Original). The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a differential signal over a pair of conductors.

16 (Original). The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously.

17 (Original). The method of claim 9 further comprising the step of:

adjusting a receiver characteristic of the receive circuit.

18 (Previously Presented). The method of claim 17 wherein the receiver characteristic is selected from a group consisting of a receiver circuit timing signal and a voltage reference.